## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for the simultaneous storage and playback of multimedia data, comprising:

an input section for acquiring an input signal;

an output section, wherein said input signal is passed to said output section as a transport stream; said output section including:

a processor;

a decoder subsystem that decodes said transport stream, said decoder subsystem connected to said processor by a first data bus; ~~and~~

a media switch connected to said decoder subsystem by a second data bus, said media switch operative to interface a plurality of system components and operates asynchronously from said processor[[.]] , wherein said media switch comprises a media manager, said media manager including:

a host controller;

a DMA controller;

a bus arbiter; and

an MPEG media stream processor; and

a storage subsystem connected to said media switch, wherein multimedia data are stored on said storage subsystem and retrieved from said storage subsystem essentially simultaneously.

2. (Original) The system of Claim 1, wherein said input section is adapted to accept an analog input signal.

3. (Previously Presented) The system of Claim 2, wherein said input section accepts said analog input signal from any of: RF coaxial, composite audio/video or S-video connectors.

4. (Previously Presented) The system of Claim 2, said input section comprising;

a tuner for selecting a desired channel;

a decoder for digitizing a video component of said input signal;

a sound processor for processing an audio component of said input signal into a digitized audio component;

an MPEG-2 encoder, wherein said MPEG-2 encoder receives digitized video and audio components, whereupon said digitized video and audio components are encoded and multiplexed into an MPEG-2 transport stream.

5. (Original) The system of Claim 4, further comprising a memory element.

6. (Previously Presented) The system of Claim 3, further comprising a secondary input, said secondary input comprising any of: a second set of RF coaxial, composite audio/video or S-video connectors.

7. (Original) The system of Claim 1, wherein said input section is adapted to accept a digital satellite input signal.

8. (Original) The system of Claim 7, wherein said input section comprises:

at least one satellite tuner; and

at least one demodulating element to demodulate the digital satellite signal to an MPEG-2 transport stream.

9. (Original) The system of Claim 1, wherein said input section is adapted to accept an input signal in both analog and digital formats from at least one RF coaxial connector.

10. (Previously Presented) The system of Claim 9, wherein said input section comprises:

at least one tuner for selecting a desired channel;

at least one decoder for digitizing a video component of said input signal;

at least one sound processor for processing an audio component of said input signal into a digitized audio component;

an MPEG-2 encoder having multi-stream encode capability, wherein said MPEG-2 encoder receives said digitized video and audio components, whereupon said digitized video and audio components are encoded and multiplexed into an MPEG-2 transport stream.

11. (Original) The system of Claim 10, further comprising at least one memory element.

12. (Original) The system of Claim 1, said output section further comprising a transport interface, wherein said transport interface receives said transport stream from said input section.

13. (Previously Presented) The system of Claim 12, said decoder further comprising an MPEG transport stream decoder/graphics subsystem.

14. (Previously Presented) The system of Claim 13, wherein said MPEG transport stream decoder/graphics subsystem includes any combination of:

a host bridge;
a memory controller;
an MPEG-2 transport demultiplexer;
an MPEG-2 decoder;
an audio/video decoder;
a graphics processor;
a bus bridge; or
a bus controller.

15. (Previously Presented) The system of Claim 14, said MPEG transport stream decoder/graphics subsystem further comprising at least one transport stream interface, wherein said transport stream interface receives said transport stream from said input section.

16. (Previously Presented) The system of Claim 14, wherein said transport stream is demultiplexed into audio and video packet streams, wherein said audio and video packet

streams are stored and played back through an output side of said MPEG transport stream decoder/graphics subsystem.

17. (Previously Presented) The system of Claim 14, wherein said MPEG transport stream decoder/graphics subsystem further comprises a plurality of outputs, wherein said decoded transport stream is output to a television, said outputs including any of:

S-video;

audio;

SPDIR (Stereo Paired Digital Interface); or

CVBS (Composite Video Baseband Signal).

18. (Previously Presented) The system of Claim 14, further comprising a SMARTCARD interface and at least one SMARTCARD reader interfaced to said MPEG transport stream decoder/graphics subsystem.

19. (Previously Presented) The system of Claim 14, further comprising a flash PROM connected to said transport stream decoder/graphics subsystem, said PROM containing boot code that initializes said system prior to loading of an operating system kernel.

20. (Original) The system of Claim 14, further comprising a SDRAM connected to said transport stream decoder/graphics subsystem.

21. (Canceled)

22. (Previously Presented) The system of Claim 1, wherein said processor comprises a MIPS processor.

23. (Original) The system of Claim 1, wherein said processor is operative to run system software, middleware, and application software.

24. (Original) The system of Claim 23, wherein said system software includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components.

25. (Canceled)

26. (Currently Amended) The system of Claim [[25]] 1, wherein said media manager is implemented in an ASIC (Application Specific Integrated Circuit) or a programmable logic device.

27. (Canceled)

28. (Canceled)

29. (Currently Amended) The system of Claim [[25]] 1, further comprising a real-time clock connected to an $I^2S$ bus.

30. (Currently Amended) The system of Claim [[25]] 1, further comprising a secure micro controller connected to a UART (Universal Asynchronous Receiver/Transmitter) included in said media manager, said micro controller operative in cryptographic applications, including authentication and encryption/decryption.

31. (Currently Amended) The system of Claim [[25]] 1, further comprising a RS232 port coupled to a UART (Universal Asynchronous Receiver/Transmitter) included in said media manager.

32. (Currently Amended) The system of Claim [[25]] 1, further comprising a IEEE1394 interface integrated on said media manager.

33. (Currently Amended) The system of Claim [[25]] 1, further comprising a front panel LED array coupled to a GPIO (General Purpose Input/Output) included in said media manager.

34. (Currently Amended) The system of Claim [[25]] 1, further comprising a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in said media manager.

35. (Currently Amended) The system of Claim [[25]] 1, further comprising a remote control coupled to an IR receiver/transmitter interface included in said media manager.

36. (Previously Presented) The system of Claim 1, wherein said second bus element comprises a system bus.

37. (Original) The system of Claim 36, wherein said system bus comprises a PCI bus.

38. (Original) The system of Claim 37, further comprising a USB (Universal Serial Bus) controller coupled to said PCI bus.

39. (Original) The system of Claim 1, wherein said system is implemented as a system board.

40. (Previously Presented) The system of Claim 1, wherein said output section is implemented as a plurality of microchips, the microchips connected to each other by said first and second bus elements.

41. (Original) The system of Claim 1, wherein said output section is implemented as either a single microchip or a chipset.

42-61. (Canceled)